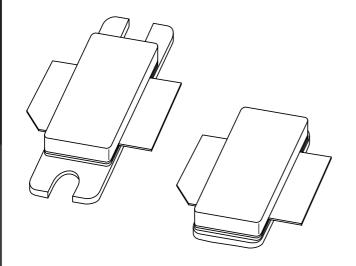
DISCRETE SEMICONDUCTORS

DATA SHEET



BLF0810-180; BLF0810S-180 Base station LDMOS transistors

Product specification Supersedes data of 2003 May 09 2003 Jun 12





Base station LDMOS transistors

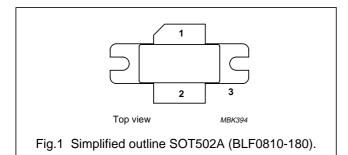
BLF0810-180; BLF0810S-180

FEATURES

- Typical CDMA IS95 performance at standard settings with a supply voltage of 27 V and I_{DO} of 1130 mA. Adjacent channel bandwidth is 30 kHz, adjacent channel at ± 750 kHz:
 - Output power = 30 W
 - Gain = 16 dB
 - Efficiency = 27%
 - ACPR = -46 dBc at 750 kHz and BW = 30 kHz
- · Easy power control
- · Excellent ruggedness
- · High power gain
- Excellent thermal stability
- Designed for broadband operation (800 to 1000 MHz)
- · Internally matched for ease of use.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



APPLICATIONS

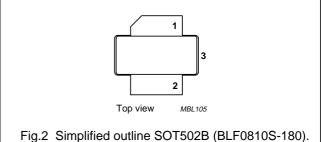
- · Common source class-AB operation applications in the 860 to 960 MHz frequency range
- CDMA and multicarrier applications.

DESCRIPTION

180 W LDMOS power transistor for base station applications at frequencies from 800 to 1000 MHz.

PINNING - SOT502B

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



QUICK REFERENCE DATA

Typical RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η _D (%)	d ₃ (dBc)	ACPR 750 (dBc)
Class-AB (2-tone)	$f_1 = 890.0; f_2 = 890.1$	27	140 (PEP)	16	39	-28	_
CDMA (IS95)	890	27	30 (AV)	16	27	_	-46

2003 Jun 12 2

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage	_	75	V
V_{GS}	gate-source voltage	_	±15	V
T _{stg}	storage temperature	-65	+150	С
Tj	junction temperature	_	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-c}	thermal resistance from junction to case	$T_h = 25 ^{\circ}C, P_L = 35 W (AV), note 1$	0.42	K/W
R _{th j-hs}	thermal resistance from heatsink to junction	$T_h = 25 ^{\circ}C, P_L = 35 W (AV), note 2$	0.62	K/W

Notes

- 1. Thermal resistance is determined under RF operating conditions.
- 2. Depending on mounting condition in application.

CHARACTERISTICS

 $T_i = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0; I_D = 3 \text{ mA}$	75	_	_	V
V _{GSth}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 300 mA	4	_	5	V
I _{DSS}	drain-source leakage current	V _{GS} = 0; V _{DS} = 36 V	_	_	3	μΑ
I _{DSX}	on-state drain current	V _{GS} = V _{GSth} + 9 V; V _{DS} = 10 V	45	_	_	Α
I _{GSS}	gate leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0$	_	_	1	μΑ
9 _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 10 A	_	9	_	S
R _{DSon}	drain-source on-state resistance	V _{GS} = 9 V; I _D = 10 A	_	60	_	mΩ

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

APPLICATION INFORMATION

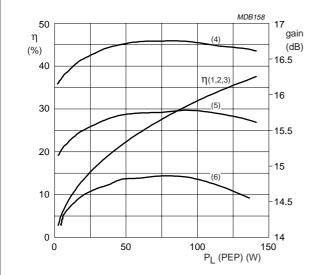
RF performance in a common source class-AB circuit.

 V_{DS} = 27 V; I_{DQ} = 1130 mA; f = 890 MHz; T_h = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mode of ope	eration: 2-tone CW, 100 kHz spacin	g	,			
G _p	gain power	P _L = 90 W (PEP)	15	16	_	dB
η_{D}	drain efficiency		24	30	_	%
IRL	input return loss		_	-13	-6	dB
d ₃	third order intermodulation distortion		_	-40	_	dBc
Gp	gain power	P _L = 125 W (PEP)	_	16	_	dB
η_{D}	drain efficiency		33	37	_	%
d_3	third order intermodulation distortion		_	-32	-27	dBc
	ruggedness	VSWR = 15 : 1 through all phases; P _L = 125 W (PEP)	no degr	adation	in output	power
Mode of ope	eration: CDMA, IS95 (pilot, paging,	sync and traffic codes 8 to 13)				
Gp	gain power	P _L = 30 W (AV)	_	16	-	dB
η_{D}	drain efficiency	P _L = 30 W (AV)	_	27	-	%
ACPR 750	adjacent channel power ratio	at BW = 30 kHz	_	-46	_	dBc

Base station LDMOS transistors

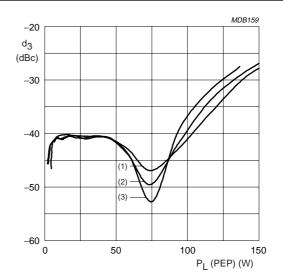
BLF0810-180; BLF0810S-180



 $V_{DS} = 27 \text{ V}; I_{DQ} = 1.1 \text{ A}; f_1 = 890.0 \text{ MHz}; f_2 = 890.1 \text{ MHz}.$

- (1) η at $T_h = -40$ °C.
- (4) gain at $T_h = -40$ °C.
- (2) η at T_h = 20 °C.
- (5) gain at $T_h = 20 \, ^{\circ}C$.
- (3) η at $T_h = 80$ °C.
- (6) gain at $T_h = 80$ °C.

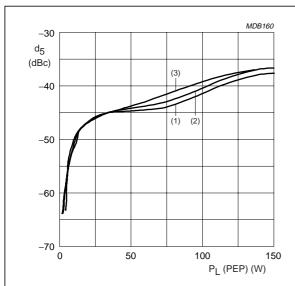
Fig.3 2-tone power gain and efficiency as functions of load power at different temperatures.



 $V_{DS} = 27 \text{ V}$; $I_{DQ} = 1.1 \text{ A}$; $f_1 = 890.0 \text{ MHz}$; $f_2 = 890.1 \text{ MHz}$.

- (1) $T_h = -40 \, ^{\circ}C$.
- (2) $T_h = 20 \, ^{\circ}C$.
- (3) $T_h = 80 \, ^{\circ}C$.

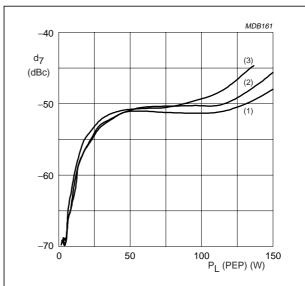
Fig.4 Third order intermodulation distortion as a function of load power at different temperatures.



 V_{DS} = 27 V; I_{DQ} = 1.1 A; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

- (1) $T_h = -40 \, ^{\circ}C$.
- (2) $T_h = 20 \, ^{\circ}C$.
- (3) $T_h = 80 \, ^{\circ}C$.

Fig.5 Fifth order intermodulation distortion as a function of load power at different temperatures.



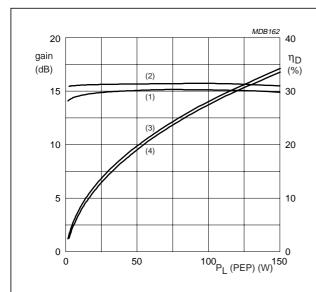
 V_{DS} = 27 V; I_{DQ} = 1.1 A; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

- (1) $T_h = -40 \, ^{\circ}C$.
- (2) $T_h = 20 \, ^{\circ}C$.
- (3) $T_h = 80 \, ^{\circ}C$

Fig.6 Seventh order intermodulation distortion as a function of load power at different temperatures.

Base station LDMOS transistors

BLF0810-180; BLF0810S-180



 $V_{DS} = 27 \text{ V}$; $f_1 = 890.0 \text{ MHz}$; $f_2 = 890.1 \text{ MHz}$.

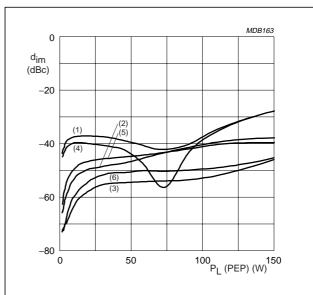
(1) $I_{DQ} = 1 A$.

(3) $I_{DQ} = 1 A$.

(2) $I_{DQ} = 1.45 A$.

(4) $I_{DQ} = 1.45 A$.

Fig.7 Power gain and drain efficiency as functions of peak envelope load power; typical values.



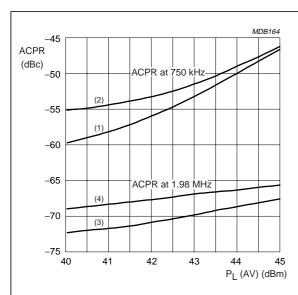
 $V_{DS} = 27 \text{ V}$; $f_1 = 890.0 \text{ MHz}$; $f_2 = 890.1 \text{ MHz}$.

(1) d_3 ; $I_{DQ} = 1 A$.

(4) d_3 ; $I_{DQ} = 1.3 A$.

(2) d_5 ; $I_{DQ} = 1$ A. (3) d_7 ; $I_{DQ} = 1$ A. (5) d_5 ; $I_{DQ} = 1.3 \text{ A}$. (6) d_7 ; $I_{DQ} = 1.3 \text{ A}$.

Fig.8 Intermodulation distortion as a function of peak envelope load power; typical values.



V_{DS} = 27 V; f = 894 MHz.

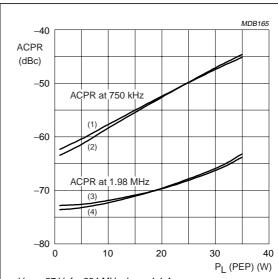
(1) $I_{DQ} = 1.1A$.

(3) $I_{DQ} = 1.1 \text{ A}.$

(2) $I_{DQ} = 1.4 A$.

(4) $I_{DQ} = 1.4 A$.

Fig.9 CDMA IS95 ACPR distortion as a function of average load power and I_{DQ}.



 $V_{DS} = 27 \text{ V}; f = 894 \text{ MHz}; I_{DQ} = 1.1 \text{ A}.$

(1) $T_h = 20 \, ^{\circ}C$.

(3) $T_h = 20 \, ^{\circ}C$.

(2) $T_h = 80 \, ^{\circ}C$.

(4) $T_h = 80 \, ^{\circ}C$.

Fig.10 CDMA IS95 ACPR distortion as a function of peak envelope load power at different temperatures.

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

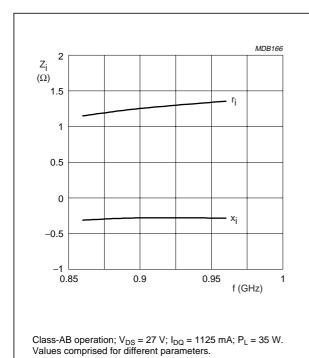
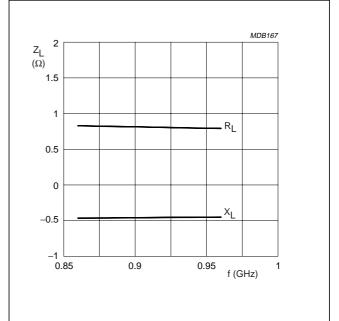
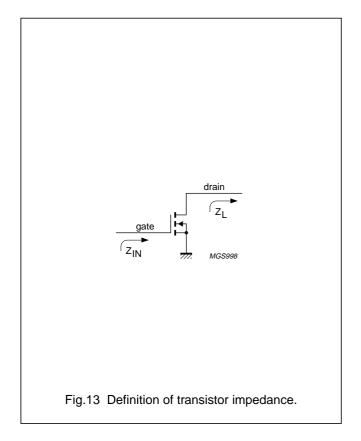


Fig.11 Input impedance as a function of frequency (series components); typical values.



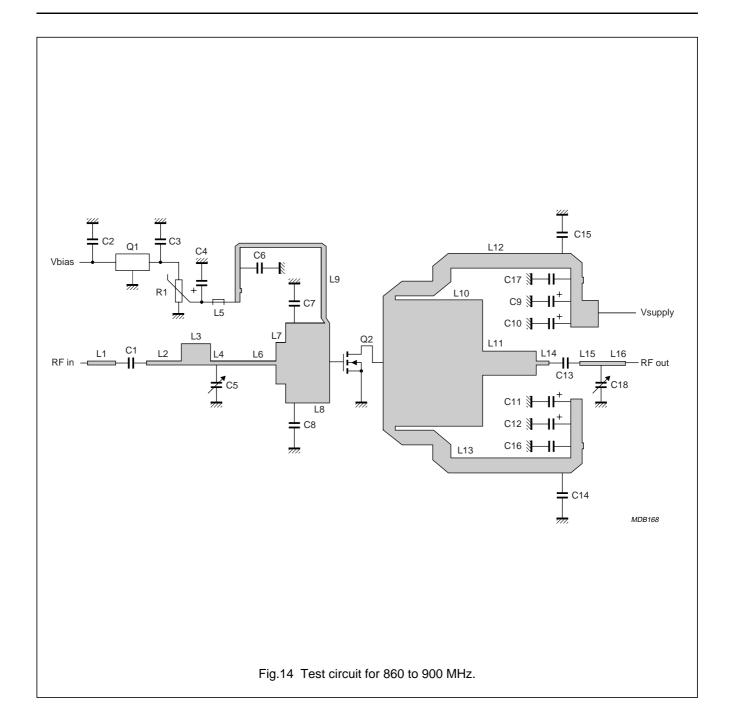
Class-AB operation; V_{DS} = 27 V; I_{DQ} = 1125 mA; P_{L} = 35 W. Values comprised for different parameters.

Fig.12 Load impedance as a function of frequency (series components); typical values.



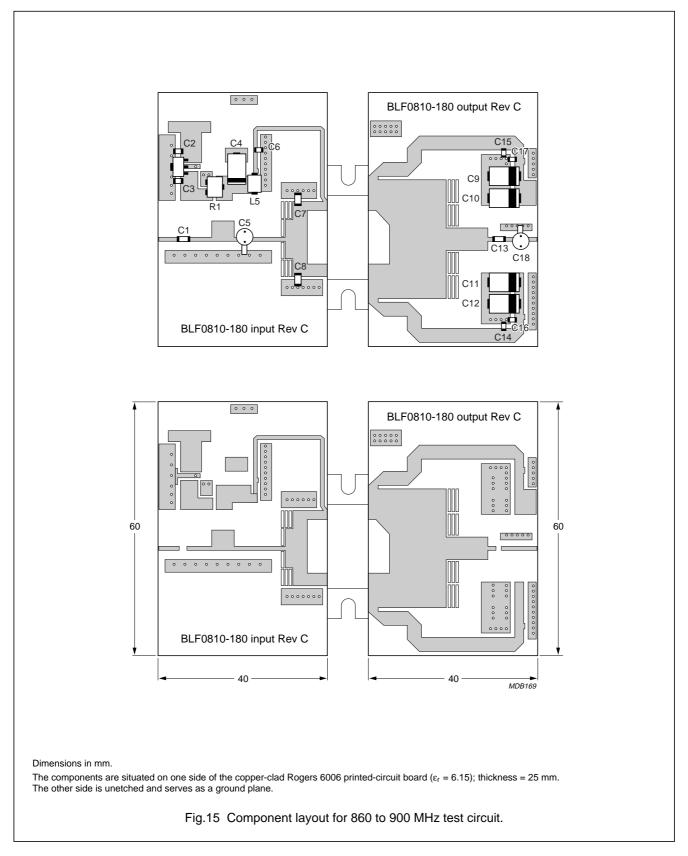
Base station LDMOS transistors

BLF0810-180; BLF0810S-180



Base station LDMOS transistors

BLF0810-180; BLF0810S-180



Base station LDMOS transistors

BLF0810-180; BLF0810S-180

List of components (see Figs 14 and 15)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF	
C2	multilayer ceramic chip capacitor; note 1	330 nF	
C3	multilayer ceramic chip capacitor; note 1	100 nF	
C4, C9, C10, C11, C12	tantalum capacitor	10 μF	
C5, C18	air trimmer capacitor	5 pF	
C7, C8	multilayer ceramic chip capacitor	8.2 pF	
R1	potentiometer	1 kΩ	
Q1	7808 voltage regulator		
Q2	BLF0810-180/BLF0810S-180 LDMOS transistor		
L1	stripline; note 2		5.22 × 0.92 mm
L2	stripline; note 2		6.47 × 0.92 mm
L3	stripline; note 2		5.38 × 4.8 mm
L4	stripline; note 2		2.4 × 0.92 mm
L5	ferroxcube		
L6	stripline; note 2		9.73 × 0.92 mm
L7	stripline; note 2		1.82 × 9.3 mm
L8	stripline; note 2		8.15 × 17.9 mm
L9	stripline; note 2		44 × 0.92 mm
L10	stripline; note 2		18.45 × 28.3 mm
L11	stripline; note 2		9.95 × 5.38 mm
L12, L13	stripline; note 2		37.6 × 3.35 mm
L14	stripline; note 2		2.36 × 0.92 mm
L15, L16	stripline; note 2		4.22 × 0.92 mm

Notes

- 1. American Technical Ceramics type 100A or capacitor of same quality.
- 2. The striplines are on a double copper-clad Rogers 6006 printed-circuit board ($\epsilon_r = 6.15$); thickness = 0.64 mm

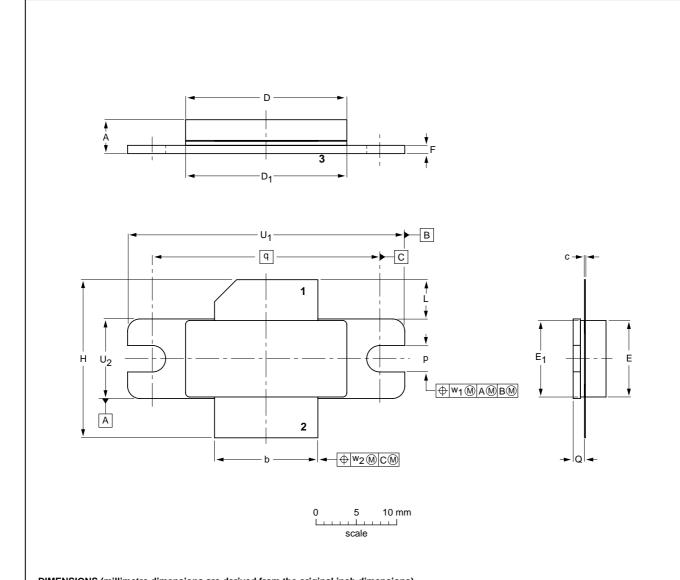
Base station LDMOS transistors

BLF0810-180; BLF0810S-180

PACKAGE OUTLINES

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A



DIMENS	SIONS (millimet	re aime	ensions	are der	ivea tro	m tne c	originai	ıncn aır	nensior	ıs)

UNIT	A	b	С	D	D ₁	E	E ₁	F	Н	L	р	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.72 3.43	12.83 12.57	0.15 0.08		19.96 19.66		9.53 9.25	1.14 0.89	19.94 18.92		3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135		0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

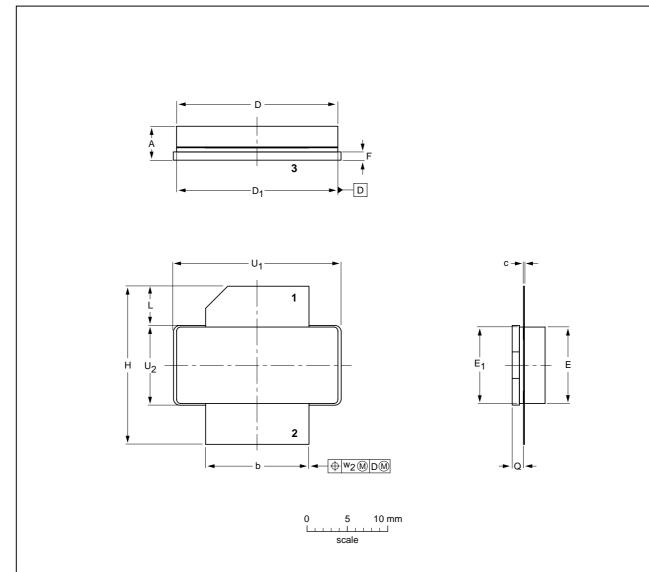
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT502A						99-12-28 03-01-10

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

Earless flanged LDMOST ceramic package; 2 leads

SOT502B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	С	D	D ₁	E	E ₁	F	Н	L	Q	U ₁	U ₂	w ₂
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135									0.210 0.170		0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT502B						99-12-28 03-01-10

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

- 1. Please consult the most recently issued data sheet before initiating or completing a design.
- 2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
- 3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

NOTES

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit http://www.semiconductors.philips.com. Fax: +31 40 27 24825 For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

© Koninklijke Philips Electronics N.V. 2003

SCA75

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

613524/06/pp16

Date of release: 2003 Jun 12

Document order number: 9397 750 11545

Let's make things better.

Philips Semiconductors



